

## REMARKS/ARGUMENTS

In the Office Action mailed on May 26, 2010, claims 1-5, 8, and 9 were rejected. Additionally, claims 6 and 7 were objected to, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, claims 1 and 9 have been amended to correct informalities. Support for the amendments to claims 1 and 9 is found in the current Application at, for example, original claims 1 and 9. Applicants hereby request reconsideration of the application in view of the claim amendments and the below-provided remarks.

### Allowable Subject Matter

Applicants appreciate the Examiner's review of the claims and determination that claims 6 and 7 recite allowable subject matter. In particular, the Office Action states that claims 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

At this time, Applicants choose not to rewrite claims 6 and 7 in independent form including all of the limitations of the base claim and any intervening claims. Instead, Applicants respectfully assert that the pending claims are allowable based on the remarks below.

### Claim Rejections under 35 U.S.C. 103

Claims 1, 2, 8 and 9 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Srikanteswara et al. (S. Srikanteswara, J.H. Reed, P. Athanas, R. Boyle, "A Soft Radio Architecture For Reconfigurable Platforms," IEEE Communications Magazine, February 2000, pages 140 -147, hereinafter "Srikanteswara") in view of Marinissen et al. (E.J. Marinissen, Y. Zorian, R. Kapur, T. Taylor, L. Whetsel, "Towards A Standard For Embedded Core Test: An Example," Proceedings of the IEEE International Test Conference, pages 616 - 627, 1999, hereinafter "Marinissen I"), and further in view of Marinissen et al. (E. Marinissen, R. Kapur, M. Lousberg, T. McLaurin,

M. Ricchetti, and Y. Zorian, "On IEEE 1500's Standard For Embedded Core Test," Journal of Electronic Testing, Volume 18, page 365-383, August 2002, hereinafter "Marinissen II"). Claims 3-5 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Srikanteswara in view of Marinissen I, further in view of Marinissen II, and further in view of Zorian et al. (Y. Zorian, E. Marinissen, S. Dey, "Testing Embedded-Core-Based System Chips," Proceedings of the IEEE International Test Conference, 1998, pages 130-143, hereinafter "Zorian"). However, Applicants respectfully submit that the pending claims are patentable over the cited references for the reasons provided below.

#### Independent Claim 1

As described above, claim 1 has been amended to correct informalities. Applicants respectfully assert that a *prima facie* case of obviousness has not been established with respect to claim 1. Specifically, Applicants respectfully assert that the articulated reasoning provided in the Office Action with respect to combining the teachings of Srikanteswara, Marinissen I, and Marinissen II is not based on a rational underpinning.

In order to establish a *prima facie* case of obviousness of a claim under 35 U.S.C. 103, the Office Action must present a clear articulation of the reason why the claimed invention would have been obvious. MPEP 2142 (citing *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007)). The analysis must be made explicit. Id. Additionally, rejections based on obviousness cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Id.

The Office Action admits that Srikanteswara does not teach:

*"linking multiplexing circuits, each linking a respective pair of stream processing circuits, each linking multiplexing circuit being individually switchable to a normal mode and to a replacement mode, the linking multiplexing circuit, when in the normal mode, providing a continuous connection for passing a first stream of samples values between the stream processing circuits in the respective pair;  
a shareable communication structure coupled to the linking multiplexing circuits, each linking multiplexing circuit, when in the replacement mode, providing a continuous connection for supplying successive sample values from a second stream*

*from the communication structure to a receiving one of the stream processing circuits in the respective pair of the linking multiplexing circuit;*

*a control circuit coupled to the linking multiplexing circuits, arranged to keep a selectable one of the multiplexing circuits in the replacement mode so that the selectable one of the linking multiplexing circuits passes a stream of successive sample from the second stream to the receiving one of the processing circuits in the respective pair of linking multiplexing circuit, while keeping at least part of the other linking multiplexing circuits in the normal mode,” as recited in claim 1. (See pages 3 and 4 of the Office Action).*

Marinissen I and Marinissen II are cited for teaching the above-identified limitations of claim 1. (See pages 5-7 of the Office Action). The Office Action suggests that the combination of Srikanteswara, Marinissen I, and Marinissen II teaches all of the limitations of claim 1. (See pages 5-7 of the Office Action).

The proposed modification of Srikanteswara in view of Marinissen I, and further in view of Marinissen II would change the principle of operation of Srikanteswara.

Applicants respectfully assert that the articulated reasoning provided in the Final Office Action is not based on a rational underpinning because the proposed modification of Srikanteswara in view of Marinissen I, and further in view of Marinissen II would change the principle of operation of Srikanteswara.

If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959) (See MPEP §2143.01 (VI)).

Srikanteswara teaches a layered radio architecture, which is a unified architecture for designing soft radios on a reconfigurable platform. (See the abstract and pages 141 and 142 of Srikanteswara). Srikanteswara also teaches that the layered radio architecture defines three layers, a soft radio interface (SRI) layer, a configuration layer underneath the SRI layer, and a processing layer underneath the configuration layer. (See Fig. 1 and pages 141 and 142, section “AN OVERVIEW OF THE LAYERED RADIO ARCHITECTURE” of Srikanteswara). In addition, Srikanteswara teaches that the configuration layer extracts configuration bits based on programming packets that are sent by the SRI layer and passes the configuration bits to the processing layer. (See Figs. 1 and 2 and page 142, section “AN OVERVIEW OF THE LAYERED RADIO ARCHITECTURE” of Srikanteswara). Furthermore, Srikanteswara teaches that the

configuration layer attaches headers to data packets from the SRI layer and sends updated data packets to the processing layer. (See page 143, section “THE CONFIGURATION LAYER” of Srikanteswara). Srikanteswara also teaches that the processing layer consists of a series of processing modules and that the processing layer configures the processing modules based on the configuration bits from the configuration layer to process the updated data packets from the configuration layer. (See Figs. 1-4, page 142, section “AN OVERVIEW OF THE LAYERED RADIO ARCHITECTURE” of Srikanteswara). In addition, Srikanteswara teaches that after completion of processing, the processing layer sends data back through the configuration layer to the SRI layer. (See Figs. 1 and 2, page 142, section “AN OVERVIEW OF THE LAYERED RADIO ARCHITECTURE,” and pages 143 and 144, section “THE PROCESSING LAYER” of Srikanteswara).

That is, Srikanteswara teaches that the processing layer of the layered radio architecture configures the series of processing modules using configuration information that is received from the soft radio interface (SRI) layer via the configuration layer, processes data that is received from the SRI layer via the configuration layer, and sends processed data back to the SRI layer via the configuration layer. Thus, the principle of operation of Srikanteswara involves configuring the series of processing modules in the processing layer of the layered radio architecture using configuration information that is received from the SRI layer via the configuration layer, processing data that is received from the SRI layer via the configuration layer using the processing modules, and sending processed data back to the SRI layer via the configuration layer.

Marinissen I teaches that a wrapper input cell includes a multiplexer, which has an input to receive information from a system chip and another input to receive scan-in test information. (See Fig. 7(b) and page 624, section “6.3 ‘1500-Compliant’ Core” of Marinissen I). Marinissen I also teaches that the multiplexer has an output to transmit the information from the system chip or the scan-in test information to a test core in the system chip. (See Fig. 7(b) and page 624, section “6.3 ‘1500-Compliant’ Core” of Marinissen I).

The Office Action states that it would have been obvious to a person of ordinary skill in the art at the time of the invention to combine the test insertion of Marinissen I with the system of Srikanteswara by linking the individual chained processors/cores of

Srikanteswara with a serial test rail and providing a multiplexing circuit for inserting and extracting test data to and from the inputs and output of each core/processor via the serial test rail while placing the remainder of the chained processors/cores in bypass mode. (See page 6 of the Office Action). The Office Action further states that the motivation to combine is provided by Marinissen I and involves allowing direct access to the inputs and output of the individual cores/processors for testing. (See pages 6 and 7 of the Office Action).

Thus, the proposed modification of Srikanteswara in view of Marinissen I would involve providing the multiplexing circuit of Marinissen I to each of the processing modules in the processing layer of Srikanteswara for inserting and extracting test data to and from the input and output of the processing module. As a result, each of the processing modules in the processing layer of Srikanteswara would receive not only the configuration information and data that are from the SRI layer via the configuration layer but also the test data through the multiplexing circuit of Marinissen I. Therefore, the configuration and the data processing of each of the processing modules in the processing layer of Srikanteswara would be interrupted by the newly added test data through the multiplexing circuit of Marinissen I.

As described above, the principle of operation of Srikanteswara involves configuring the series of processing modules in the processing layer of the layered radio architecture using configuration information that is received from the SRI layer via the configuration layer, processing data that is received from the SRI layer via the configuration layer using the processing modules, and sending processed data back to the SRI layer via the configuration layer. Because the proposed modification of Srikanteswara in view of Marinissen I would result in the configuration and the data processing of each of the processing modules in the processing layer of Srikanteswara being interrupted by the newly added test data through the multiplexing circuit of Marinissen I, Applicants respectfully assert that the proposed modification of Srikanteswara in view of Marinissen I would change the principle of operation of Srikanteswara.

In addition, Applicants respectfully assert that combining the teachings of Srikanteswara as modified by Marinissen I with Marinissen II does not remedy the

above-identified problem. Thus, combining the teachings of Srikanteswara as modified by Marinissen I with Marinissen II would change the principle of operation of Srikanteswara.

The proposed modification of Srikanteswara in view of Marinissen I, and further in view of Marinissen II would render Srikanteswara unsatisfactory for its intended purpose.

In addition, Applicants respectfully assert that the articulated reasoning provided in the Final Office Action is not based on a rational underpinning because the proposed modification of Srikanteswara in view of Marinissen I, and further in view of Marinissen II would render Srikanteswara unsatisfactory for its intended purpose.

If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984) (see MPEP §2143.01(V)).

As described above, Srikanteswara teaches that the processing layer of the layered radio architecture configures the series of processing modules using configuration information from the SRI layer through the configuration layer, processes data from the SRI layer through the configuration layer, and sends processed data back to the SRI layer through the configuration layer. That is, the intended purpose of Srikanteswara is to use the series of processing modules in the processing layer to process data from the SRI layer based on configuration information from the SRI layer.

As described above, the proposed modification of Srikanteswara in view of Marinissen I would result in the configuration and the data processing of each of the processing modules in the processing layer of Srikanteswara being interrupted by the newly added test data through the multiplexing circuit of Marinissen I. As a result, the proposed modification of Srikanteswara in view of Marinissen I would render Srikanteswara unsatisfactory for using the series of processing modules in the processing layer to process data from the SRI layer based on configuration information from the SRI layer. Thus, the proposed combination of Srikanteswara and Marinissen would render Srikanteswara unsatisfactory for its intended purpose.

In addition, Applicants respectfully assert that combining the teachings of Srikanteswara as modified by Marinissen I with Marinissen II does not remedy the above-identified problem. Thus, combining Marinissen II with the teachings of Srikanteswara as modified by Marinissen I would render Srikanteswara unsatisfactory for its intended purpose.

Accordingly, combining the teachings of Srikanteswara as modified by Marinissen I with Marinissen II would change the principle of operation of Srikanteswara and render Srikanteswara unsatisfactory for its intended purpose. Thus, Applicants respectfully assert that the articulated reasoning provided in the Office Action is not based on a rational underpinning. Because the articulated reasoning provided in the Office Action is not based on a rational underpinning, Applicants respectfully assert that a *prima facie* case of obviousness has not been established with respect to claim 1. As a result, Applicants respectfully submit that claim 1 is patentable over Srikanteswara in view of Marinissen I, and further in view of Marinissen II.

#### Dependent Claims 2-8

Claims 2-8 depend from and incorporate all of the limitations of independent claim 1. Applicants respectfully assert that claims 2-8 are allowable at least based on an allowable claim 1.

#### Independent Claim 9

Claim 9 includes similar limitations to claim 1. Because of the similarities between claim 1 and claim 9, Applicants respectfully assert that the above remarks with regard to claim 1 apply also to claim 9. Accordingly, Applicants respectfully assert that claim 9 is patentable over Srikanteswara in view of Marinissen I, and further in view of Marinissen II.

## CONCLUSION

Applicants respectfully request reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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